What Is Claimed Is:

1. A semiconductor device comprising:

a semiconductor chip having over a main surface thereof an integrated circuit and plural electrodes;

plural leads having end portions on one side fixed to a back surface of said semiconductor chip and opposite end portions used as external terminals;

plural wires for connecting the plural electrodes on said semiconductor chip with the plural leads positioned outside said semiconductor chip;

and

a resin sealing member for sealing said semiconductor chip, portions of said plural leads and said plural wires, the opposite end portions of said plural leads being exposed from a back surface of the resin sealing member.

2. The semiconductor device according to claim 1, wherein said external terminals comprise first external terminals arranged along side faces of the resin sealing member and second external terminals arranged inside said first external terminals and each disposed between adjacent ones of said first external terminals.

3. The semiconductor device according to claim 1,

wherein the plural leads comprise plural first leads end portions on one side of which are positioned outside

said semiconductor chip and plural second leads each disposed between adjacent ones of said first leads and end portions on one side of which are fixed to the back surface of the semiconductor chip,

wherein said plural first leads include said first external terminals respectively, and

wherein said plural second leads include said second external terminals respectively.

4. The semiconductor device according to claim 1, further comprising a spacer fixed to an upper surface of said semiconductor chip and exposed partially from an upper surface of said resin sealing member.

5. A semiconductor device comprising:

an insulating base;

a semiconductor chip having over a main surface thereof an integrated circuit and plural electrodes, the semiconductor chip being fixed over said insulating base;

plural leads end portions on one side of which are fixed to said insulating base and opposite end portions of which are used as external terminals;

plural wires for connecting the plural electrodes formed on said semiconductor chip with said plural leads positioned outside said insulating base; and

a resin sealing member for sealing said insulating

base, said semiconductor chip, portions of said plural leads and said plural wires, the opposite end portions of said leads being exposed from a back surface of the resin sealing member.

6. The semiconductor device according to claim 5, wherein said external terminals comprise first external terminals arranged along side faces of the resin sealing member and second external terminals arranged inside said first external terminals and each disposed between adjacent ones of said first external terminals.

7. The semiconductor device according to claim 6,

wherein said plural leads comprise plural first leads end portions on one side of which are positioned outside said insulating base and plural second leads each disposed between adjacent ones of said first leads and end portions on one side of which are fixed to said insulating base,

wherein said plural first leads include the first external terminals respectively, and

wherein said plural second leads include said second external terminals respectively.

8. The semiconductor device according to claim 5, further comprising a spacer fixed to an upper surface of said semiconductor chip and exposed partially from an upper surface of said resin sealing member.

9. A method of manufacturing a semiconductor device having external terminals formed by exposing leads partially from a back surface of a resin sealing member, the method comprising the steps of:

(a) providing a semiconductor chip and plural leads, the semiconductor chip having over a main surface thereof an integrated circuit and plural electrodes;

(b) fixing end portions on one side of said plural leads to a back surface of said semiconductor chip;

(c) connecting portions of said plural leads positioned outside said semiconductor chip with the electrodes formed over said semiconductor chip through plural wires;

(d) forming a spacer over an upper surface of said semiconductor chip; and

(e) sealing said semiconductor chip, said plural leads and said plural wires with a resin sealing member,

said resin sealing member being formed by a transfer molding method involving injection of resin into a cavity of a molding die, and

said resin sealing member being formed by injecting said resin in a state in which a part of said spacer is in contact with an inner surface of the cavity of the molding die.

10. The method of manufacturing a semiconductor

device according to claim 9,

wherein said semiconductor chip is one of plural semiconductor chips obtained by dicing a semiconductor wafer, and

wherein said spacer is formed over each of said plural semiconductor chips in a state of said semiconductor wafer prior to the dicing of said semiconductor wafer.

11. The method of manufacturing a semiconductor device according to claim 10, wherein said spacer is formed of a silicon piece.

12. The method of manufacturing a semiconductor device according to claim 11, wherein said silicon piece is one of plural silicon pieces obtained by dicing a silicon wafer and which further comprises the steps of affixing said silicon wafer over said semiconductor wafer prior to the dicing of said silicon wafer, and subsequently dicing said silicon wafer.

13. The method of manufacturing a semiconductor device according to claim 10, wherein said spacer is formed by an insulating layer, and said insulating layer is formed by printing.

14. The method of manufacturing a semiconductor device according to claim 13, wherein said insulating layer is a polyimide layer.

15. A method of manufacturing a semiconductor device having external terminals formed by exposing leads partially from a back surface of a resin sealing member, the method comprising the steps of:

(a) providing a semiconductor chip and plural leads end portions on one side of which are fixed to an insulating base, the semiconductor chip having over a main surface thereof an integrated circuit and plural electrodes;

(b) fixing the semiconductor chip over said insulating base;

(c) connecting portions of the plural leads positioned outside said semiconductor chip with the electrodes formed on said semiconductor chip through plural wires;

(d) forming a spacer over an upper surface of said semiconductor chip; and

(e) sealing said semiconductor chip, said insulating base, said plural leads and said plural wires with a resin sealing member,

said resin sealing member being formed by a transfer molding method involving injection of resin into a cavity of a molding die, and said resin sealing member being formed by injection of said resin in a state in which a part of said spacer is in contact with an inner surface of the cavity of the molding die.

16. A method of manufacturing a semiconductor device having plural semiconductor chips over a wiring substrate, the method comprising the steps of:

(a) providing first and second semiconductor chips each having an integrated circuit and plural electrodes;

(b) mounting said first semiconductor chip over a main surface of said wiring substrate;

(c) stacking said second semiconductor chip over said first semiconductor chip through a spacer;

(d) connecting the electrodes formed over each of said first and second semiconductor chips with plural terminals arranged over the main surface of said wiring substrate through plural wires; and

(e) sealing said first and second semiconductor chips and said wires with a resin sealing member over the main surface of said wiring substrate,

said first semiconductor chip being one of plural semiconductor chips obtained by dicing a semiconductor wafer,

said spacer being formed over each of said plural semiconductor chips in a state of said semiconductor wafer prior to the dicing of said semiconductor wafer, and

said step (b) including a step of mounting said first semiconductor chip with said spacer formed over it over the

main surface of said wiring substrate.

17. The method according to claim 16, further comprising a step of grinding and spin etching a back surface of said semiconductor wafer to reduce a thickness of the semiconductor wafer,

wherein said spacer is mounted over said semiconductor wafer after the step of reducing the thickness of said semiconductor wafer.

18. A method of manufacturing a semiconductor device having plural semiconductor chips over a chip mounting portion of a lead frame, the method comprising the steps of:

(a) providing first and second semiconductor chips each having an integrated circuit and plural electrodes;

(b) mounting said first semiconductor chip over said chip mounting portion;

(c) stacking said second semiconductor chip over said first semiconductor chip through a spacer;

(d) connecting the electrodes formed over each of said first and second semiconductor chips with plural leads formed over said lead frame through plural wires; and

(e) sealing said chip mounting portion, portions of said plural leads, said first and second semiconductor chips and said plural wires with a resin sealing member,

said first semiconductor chip being one of plural semiconductor chips obtained by dicing a semiconductor wafer,

said spacer being formed over each of said plural semiconductor chips in a state of said semiconductor wafer prior to the dicing of the semiconductor wafer, and

said step (b) including a step of mounting said first semiconductor chip with said spacer formed over it over said chip mounting portion.

19. The method according to claim 18, further comprising a step of grinding and spin etching a back surface of said semiconductor wafer to reduce the thickness of the semiconductor wafer,

wherein said spacer is mounted over said semiconductor wafer after the step of reducing the thickness of said semiconductor wafer.